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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,268	10/22/2001	Jeng-Jye Shau	SHAU-0103	8393

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UNIRAM TECHNOLOGY, INC.
3375 SCOTT BLVD.
336
SANTA CLARA, CA 95054

EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/038,268	SHAU, JENG-JYE	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *1-10,15 and 16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/25/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 1-10, 15 and 16 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected inventions, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/15/2004.

Drawings

2. The drawings were received on 10/22/2001. These drawings are accepted.

Specification

3. The abstract was received on 08/19/2005. The abstract was accepted.

Response to Arguments

4. Applicant's arguments with respect to claims 11-14 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

The Examiner suggests the following changes to claim 1 to remove minor grammatical problems:

--an error-check logic circuit connected to said memory-cell array for checking errors of said data access to said memory-cell arrays wherein said error-check logic circuit further includes an array of identical parity-check circuit blocks, P[i], where i=1,2,3...,K and K is a positive integer and said identical parity-check circuit blocks **perform** a parity check on a rotational relationship with each P[i] circuit block receiving input data from a P[i-1] circuit block and sending output to a P[i+1] circuit block while said P[K] circuit block **sends** output data to said P[1] circuit block--.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freeman; Richard B. et al. (US 3678469 A, hereafter referred to as Freeman) in view of Chang; Chih-Wei D. et al. (US 5455834 A, hereafter referred to as Chang).

35 U.S.C. 103(a) rejection of claim 11.

Freeman teaches an error-check logic circuit further includes an array of identical parity-check circuit blocks represented by P[i] where i=1,2,3...,K and K is a positive integer (The Rectangular Parity Check Array in Figure 4 and 1 of Freeman is comprised of N=8 rows of identical parity-check circuit blocks represented by R[s] where s=0,1,2,3...,N-1; Note: if i=s+1, P[i]=R[s+1] and K=N, then the rows of identical parity-check circuit blocks are identical to those of the Applicant's claim 10) and said identical parity-check circuit blocks performing a parity check on a rotational relationship with each of said P[i] circuit block receiving input data from a P[i-1] circuit block and sending output to a P[i+1] circuit block (Note each P[i] row circuit block in Freeman receives input data on the 3rd input line of the P[i] row circuit block from the P[i-1] row circuit block and sends output to the 3rd input line of the P[i+1] row circuit block) while said P[K] circuit block sending ding output data to said P[1] circuit block (Figure 1 in Freeman teaches that CRC output from the last P[K] row circuit block is recirculated vian Memory 14 and Old CRC register 24 as input to the first P[1] row circuit block). In addition, Freeman teaches the error-check logic circuit connected to a memory 14 in Figure 1 of Freeman for checking errors. However Freeman does not explicitly teach the specific use of the error-check logic circuit taught in Freeman for checking errors of said data access to a memory-cell array. Chang, in an analogous art, teaches use of an error-check logic circuit for checking errors of said data access to a memory-cell array (Figure 3 in Chang teaches a CAM device 24 comprising various arrays for addresses 80, Data 94, error detection and

correction parity bits 96 & 98 and validation bits 100; Error processors 48A & 48B are error-check logic circuits for checking errors of said data access to each of said memory-cell arrays by verifying both data and address content).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Freeman with the teachings of Chang by including use of the error-check logic circuit taught in Freeman for checking errors of said data access to a memory-cell array. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the error-check logic circuit taught in Freeman for checking errors of said data access to a memory-cell array would have provided for detecting and handling hardware errors in a memory table (see Abstract in Chang).

35 U.S.C. 103(a) rejection of claims 12-14.

Chang teaches parity bit arrays 96 & 98 in Figure 3 of Chang for storing an error-code check (ECC) parity for each of said memory-cell array used by said error-check logic circuit for checking errors of said data access to each of said memory-cell arrays. Note: Figure 4 is a circuit for generating an EDC check bit for storage in a memory cell of bit arrays 96 & 98 in Figure 3 of Chang. Note also SRAM is RAM.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11

F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 11-14 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of U. S. Patent No. US 6216246 B1 in view of Chang; Chih-Wei D. et al. (US 5455834 A, hereafter referred to as Chang).

Double patenting rejection of claim 11.

Claim 1 of U. S. Patent No. US 6216246 B1 teaches an error-check logic circuit connected to said memory-cell array for checking errors of said data access to said memory-cell arrays wherein said error-check logic circuit further includes an array of identical parity-check circuit blocks, P[i], where i=1,2,3...,K and K is a positive integer and said identical parity-check circuit blocks **perform** a parity check on a rotational relationship with each P[i] circuit block receiving input data from a P[i-1] circuit block and sending output to a P[i+1] circuit block while said P[K] circuit block **sends** output data to said P[1] circuit block.

However claim 1 of U. S. Patent No. US 6216246 B1 does not explicitly teach the specific use of the error-check logic circuit taught in claim 1 of U. S. Patent No. US 6216246 B1 for checking errors of said data access to a memory-cell array.

Chang, in an analogous art, teaches use of an error-check logic circuit for checking errors of said data access to a memory-cell array (Figure 3 in Chang teaches a CAM device 24 comprising various arrays for addresses 80, Data 94, error detection and correction parity bits 96 & 98 and validation bits 100; Error processors 48A & 48B are error-check logic circuits for checking errors of said data access to each of said memory-cell arrays by verifying both data and address content).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claim 1 of U. S. Patent No. US 6216246 B1 with the teachings of Chang by including use of the error-check logic circuit taught in claim 1 of U. S. Patent No. US 6216246 B1 for checking errors of said data access to a memory-cell array. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the error-check logic circuit taught in Freeman for checking errors of said data access to a memory-cell array would have provided for detecting and handling hardware errors in a memory table (see Abstract in Chang).

Double patenting rejection of claims 12-14.

Chang teaches parity bit arrays 96 & 98 in Figure 3 of Chang for storing an error-code check (ECC) parity for each of said memory-cell array used by said error-check logic

circuit for checking errors of said data access to each of said memory-cell arrays. Note: Figure 4 is a circuit for generating an EDC check bit for storage in a memory cell of bit arrays 96 & 98 in Figure 3 of Chang. Note also SRAM is RAM.

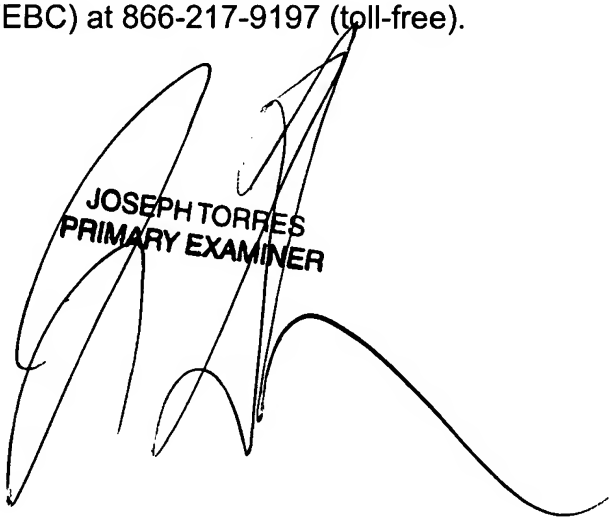
Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133